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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/800,213	03/06/2001	John Howard Coleman		4985

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EXAMINER	
TRAN, MINH LOAN	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/800,213	COLEMAN, JOHN HOWARD	
	Examiner	Art Unit	
	Minh-Loan T. Tran	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/11/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II, claims 1-12 in the reply filed on 06/16/2003 is acknowledged.

Information Disclosure Statement

2. The information disclosure statement filed 04/11/2001 has been considered.

Oath/Declaration

3. The oath or declaration filed on 03/06/2001 is acceptable.

Drawings

4. The drawings are objected to because figures 3, 4, 8-10 have such faint lines and the reference numerals that the specification cannot be read on the drawings. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the

drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The disclosure is objected to because of the following informalities:

On page 6, paragraph [0026], line 9, "surface layer **12**" should be changed to –surface layer **11**—for clarity.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, lines 8 and 9, "said device region" is unclear as to whether it is being referred to the p-type device region.

In claim 10, lines 1 and 2, "forming a CMOS structure in **said device region**" is unclear as to whether it is being referred to the p-type region. Note that CMOS structure (PMOS and NMOS) is formed in layer 1 which has p-type region (NMOS) and n-type region (PMOS).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. (Properties of Silicon-on-Defect-Layer material, Material Research Society, Vol. 396, pages 745-750, 1995) in view of Grisolia et al. (A transmission electron microscopy quantitative study of the growth kinetics of H platelets in Si, Applied Physics Letters, Vol 76, No. 7, Feb. 2000.)

With regard to claims 1 and 7, pages 746 and 747 of Li et al. discloses a method for making a semiconductor device having a p-type region, comprising the steps of :
(i) forming an initial region to an initial depth from at least a portion of an initial surface of a semiconductor substrate which has n-type conductivity and an original bulk spreading resistivity (40 Ω-cm);
(ii) heating the initial region, therein to develop an initial spreading resistivity profile having a peak, with peak value greater than the bulk spreading resistivity (see figure 1 of Li et al.)

Li et al. does not disclose the step of removing from the initial surface portion thereby forming the device region having a new surface from which the resistivity peak is at a reduced depth. However, page 852, right column, lines 12 and 13 of Grisolia et al. disclose that removing a surface of a wafer is a standard procedure for thinning the semiconductor wafer after the proton is implanted and annealed. Therefore, it would have been obvious to one of ordinary skill in the art to remove the initial surface portion of Li et al. so that the device region having a new surface from which the resistivity peak

is at a reduced depth such as taught by Grisolia et al., because such process step is a standard procedure for thinning the semiconductor wafer.

With regard to claims 2 and 3, Li et al. discloses step (i) comprises implanting particles, wherein the particles are hydrogen ions (page 746.)

With regard to claim 4, Grisolia et al. discloses the p-type silicon wafer were proton implanted with a dose of a few 10^{16} H^+ cm^{-2} (note right column on page 852 of Grisolia et al.)

With regard to claims 5 and 6, page 746 of Li et al. discloses the substrate has n-type conductivity and wherein in step (ii), heating results in a change of conductivity to p-type in the initial region and the heating for changing the n-type conductivity type to p-type conductivity type is distinct from heating to develop the initial spreading resistivity profile.

With regard to claims 8-10, the Abstract and page 749 of Li et al. disclose that the SODL (Silicon-on-Defect-Layer) material is suitable for forming CMOS device.

With regard to claim 11, the Abstract of Li et al. discloses a trench between NMOS and PMOS having a depth of at least to the depth of the peak of the spreading resistivity of the device region, because Li et al. states that the p-n junction in SODL material functions as an isolation of a well in a CMOS device.

With regard to claim 12, Li et al. and Grisolia et al. do not disclose a step of growing a crystalline region on the device region. However, it would have been obvious to one of ordinary skill in the art to grow the crystalline region on the device region of Li

et al. and Grisolia et al. because such structure is conventional in the art for forming the CMOS device having high electron mobility.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh-Loan T. Tran whose telephone number is (571) 272-1922. The examiner can normally be reached on Monday-Friday 9:00 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mlt
12/04

Minh-Loan T. Tran
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Art Unit 2826